



JRW
PATENT
8008-1052

IN THE U.S. PATENT AND TRADEMARK OFFICE

In re application of

Yasutaka NAKASHIBA

Conf. 2273

Application No. 10/812,282

Group 2815

Filed March 30, 2004

Examiner J. Fenty

SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In compliance with Rules 1.97 and 1.98, and in fulfillment of the duty of disclosure under Rule 1.56, the accompanying document, a copy of which is attached to this statement, is made of record on the enclosed Form PTO-1449.

A concise explanation of the relevance of this item is that this reference was cited by the Chinese Patent Office in an Official Action. A copy of the Chinese Official Action (with English translation) in which it was cited is attached hereto.

Under the provisions of 37 CFR 1.97(e), the undersigned hereby certifies that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign Patent Office in a

counterpart foreign application not more than three months prior to the filing of this Statement.

Respectfully submitted,

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March 15, 2006



EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

* Abstract provided for the Examiner's convenience